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May 28, 1959

RE W18-59

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Dear Mr. [redacted]

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In response to the verbal request of Messrs. [redacted] and [redacted], the [redacted] hereby submits for your approval the attached Proposal B-287-B, re your requirement W18-59 [redacted].

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As indicated in the Proposed Development Schedule, the prototype unit will be delivered for evaluation by the end of the ninth month following date of award of contract.

It is estimated that the total cost for this program is approximately $128,000. Of this amount, $80,000 is the estimated cost of the research and development of the prototype unit. The subsequent four final models are estimated at $11,000 each. Actual fabrication time for these units will take four months.

Very truly yours,

[redacted]

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Manager
Ballistic Missile Division

rda

[redacted]

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[redacted]

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B-287-B

The [redacted] proposes to develop [redacted] 25X1 25X1

Memory Units to suit Task Outline No. 59-A-1091-A dated 19 May 1959. Approximate time and cost estimates are provided for planning purposes as specifically applied to the delivery of one prototype unit. After the evaluation of this unit it is anticipated that four additional units of a preproduction nature will be contracted for separately. The proposal is based upon the assumption that any contract which might be negotiated would be of the CPFF type and contain the normal provisions required by the Armed Services Procurement Regulation.

Since the preliminary discussions and subsequent receipt of the specifications, a study of the problem makes clear the desirability of using ferrite cores in preference to Twistors for the basic storage element. The section of the proposal on technical approach develops this comparison in detail and describes the miniaturized packaging to be employed.

The proposed technique exceeds the specification by providing twice the specified memory capacity in the required volume and allows the shortest possible development cycle.

Technical Discussion

The memory as proposed will accept six input lines of data and store in serial fashion each bit in a ferrite memory plane. Read and write operations will be accomplished by a selection technique wherein a negative 1/3 current bias is applied to all cores and the selected core is at the

intersection of x and y currents of 2/3 amplitude. By using this technique, the noise level from the memory is reduced, the tolerance on current pulse levels is relaxed by comparison with usual coincident current systems and the temperature spread of operation drastically improved. Addressing of the memory location will be under the control of a counting register. In this way the memory can be loaded and unloaded in serial order. If required, the counter may be made to reverse the order of operation. By means of presetting the counter, the operation may be made to start at any predetermined point. Provision is made in the logic to negate the transfer of characters to the memory during the periods when all zeros are coming in. This provision also ensures synchronism with the source. Figure 1 shows a block diagram of the Proposed System.

There are a number of operating memories using 1/3 and 2/3 partial current, in particular one at the [redacted] and one at the [redacted] production plant containing 512 words of 32 bits each, that are "worst case" designed for an operating range of from 0°C to +55°C. Current regulation requirements were relaxed to a ± 15% margin for the above performance. Since Twistors have not been proven amenable to this technique, the two advantages of relaxed current regulation and increased temperature range when using ferrite cores are considered highly desirable for the proposed memory element. 25X1 25X1

A critical examination was made of the lead time requirements for producing both a Twistor and a ferrite core memory package. The ready availability of ferrite cores and the use of existing and reliably proven circuit and packaging techniques already associated with the cores provides a reduction

of total development time by a factor of approximately two over that obtainable with Twistors.

Although the [redacted] Twistor memory development has full support and high priority within the Corporation, the effort to date has been towards producing the destructive version of the Twistor as opposed to the non-destructive type. The basic phenomena of the Twistor is such that it does not appear feasible to package the 1800 bit Twistor Memory within the specified volume. At the present state of the art, Twistor memory cells interact unfavorably if the distance between elements is decreased beyond certain limits.

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In contrast, a recent development in high density packaging of small 30 mil by 50 mil ferrite cores can be applied directly to the proposed memory unit. This core technique was developed for the AN/ASB-6 Airborne Computer, and when coupled with miniature packaging techniques allows twice the memory capacity called for in the specifications while retaining the desired form factor.

In summary, the ferrite core memory as described above is proposed in lieu of the Twistor technique for reasons of (1) shortened development time, (2) proven circuit reliability, (3) higher memory packaging density, and (4) guaranteed environmental capability.

Packaging

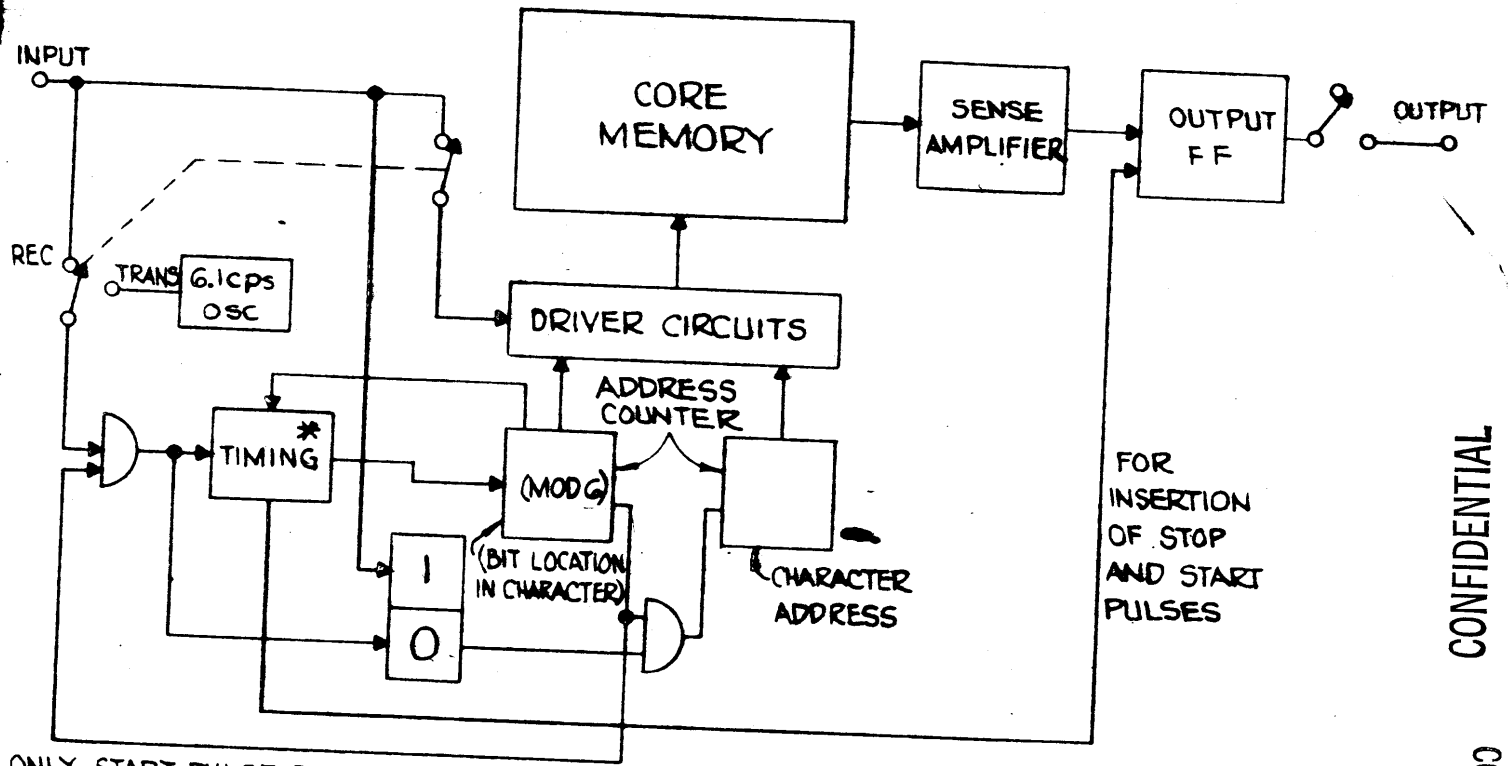
In view of the request for the use of military approved components and the time schedule for the fabrication of the first unit, a modification of

the circuit packaging technique now being used for the airborne computer will be employed here. The electronics circuitry, control and logic, will be packaged in plaques. In general only one circuit, such as a complete flip-flop, will be in each plaque. The memory core will be packaged as a separate unit. By using unitized construction the system functions, capacity, and form factor may be altered without major changes.

The circuit plaque or CHIP (circuit holding and integrating plaque) is precast as a shell with the connector and some of the circuit wiring formed in place. The shell also acts as a jig for holding the components during assembly. After assembly the chips and memory plane will be arranged as shown in Figure 2. The overall dimension of the chip is 0.9 x 0.45 x 0.15 inches and can contain on the order of 21 components. It is estimated that the overall component density of the Final Memory Unit will be approximately 100 to the cubic inch, a requirement that is well within the state of the art.

As mentioned earlier, the core stick is proposed. Since the magnetic field is contained completely within the core, magnetic flux interference does not become a factor in achieving high density packaging. A core plane containing 1800 cores will measure 0.1 x 2¼ x 4½ inches. Two such planes will be used to provide the 3600 bit storage capacity proposed.

The design and layout of the system for the prototype model will be made so that printed circuit cards can be used for the interconnection of the chips. The first model, however, will be hand wired and employ welded connections wherever possible. By using this technique, system changes as a result of operational evaluation or requirement changes can be accomplished with a minimum of delay.



ONLY START PULSE PERMITTED TO OPERATE TIMING (FOR SYNCHRONIZATION)

CARRY IN ADDRESS COUNTER PERMITTED TO CHANGE WRITING TO NEXT CHARACTER ONLY IF CHARACTER INSERTED IS NOT IDLING CHARACTER.

*G PULSES COUNTED BY FAST END OF ADDRESS COUNTER

TRANSMIT-RECEIVE SWITCH IS 3 POLE SWITCH. ELECTRONIC SWITCHING CONTROLLED BY PUSH-BUTTON CONTROL WILL BE USED.

Fig. 1

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SOLID STATE MEMORY UNIT

Fig. 2.

PROPOSED DEVELOPMENT SCHEDULE